AMENDMENTS TO THE CLAIMS

The listing of claims below replace all prior versions, and listings, of claims:

1   1.   (Currently Amended) A system comprising:

2   a memory bus; and

3   a plurality of memory controllers, each memory controller to generate

4 memory requests on the memory bus according to a predetermined priority scheme, the

5 predetermined priority scheme defining time slots, wherein the memory controllers are

6 allocated to respective time slots according to the predetermined priority scheme,

7   at least two of the plurality of memory controllers adapted to generate

8 concurrently pending memory requests on the memory bus in plural respective time slots.

1   2.   (Cancelled)

1   3.   (Cancelled)

1   4.   (Original) The system of claim 1, wherein the memory bus comprises a

2 Rambus channel.

1   5.   (Original) The system of claim 1, wherein each memory controller

2 generates a memory request during a different predetermined time slot.

1   6.   (Original) The system of claim 1, wherein the memory bus comprises

2 plural control portions, each of the control portions associated with corresponding time

3 slot priority schemes.

1   7.   (Original) The system of claim 6, wherein the time slot priority schemes

2 are staggered.

1   8.   (Original) The system of claim 6, wherein the control portion comprise a

2   row portion and a column portion.

1   9.   (Original) The system of claim 1, wherein the memory bus comprises

2   plural portions, each portion associated with a set of memory devices.

1   10.   (Currently Amended) A system comprising:

2   a plurality of memory buses bus; and

3   a hub connected to the plurality of memory buses; and

4   a plurality of memory controllers connected to a first one of the memory

5   bus buses, each memory controller to monitor memory requests generated by another

6   memory controller in performing memory-related actions,

7   the memory controllers to access a second one of the memory buses

8   through the hub.

1   11.   (Original) The system of claim 10, wherein the memory-related actions

2   comprise a read-modify-write transaction.

1   12.   (Original) The system of claim 10, wherein the memory-related actions

2   comprise a cache coherency action.

1   13.   (Original) The system of claim 10, wherein the memory-related actions

2   comprise a memory request.

1   14.   (Currently Amended) The system of claim 10, the each memory controller

2   to determine if the memory buses are bus is available based on outstanding requests from

3   other memory controllers.

1   15.   (Currently Amended) A method <u>for use in a system having plural memory</u>

2   <u>buses, a hub connected to the memory buses, and a plurality of memory controllers, the</u>

3   <u>method</u> comprising:

4   ~~providing multiple memory controllers on a memory bus;~~

5   generating requests, by the memory controllers, on the memory ~~bus~~ <u>buses</u>;

6   and

7   each memory controller monitoring memory-related actions <u>on the</u>

8   <u>memory buses connected by the hub</u> by at least another memory controller.

1   16.   (Original) The method of claim 15, wherein generating the requests

2   comprises generating Rambus command packets.

1   17.   (Original) The method of claim 15, wherein generating the requests

2   comprises the memory controllers generating the requests one at a time according to a

3   predetermined priority scheme.

1   18.   (Original) The method of claim 17, wherein generating the requests

2   comprises generating the requests according to a time slot priority scheme.

1   19.   (Original) The method of claim 17, wherein generating the requests

2   comprises generating the requests according to a request-select priority scheme.

1   20.   (Previously Presented) The method of claim 15, further comprising each

2   memory controller determining when to generate a memory request based on the

3   monitoring.

1   21.   (Previously Presented) The method of claim 15, further comprising each

2   memory controller determining if a lock has been asserted due to presence of a read-

3   modify-write transaction.

1   22.   (Previously Presented) The method of claim 15, further comprising each

2   memory controller performing a cache coherency action based on the monitoring.

1   23.   (Currently Amended) An article comprising one or more storage media

2   containing instructions that when executed cause a memory controller to:

3   monitor memory requests from another memory controller on a memory

4   bus;

5   ~~determining~~ determine if a memory request can be generated on the

6   memory bus based on the monitoring; and

7   generate memory requests on the memory bus according to a time slot

8   priority scheme that defines time slots allocated to respective memory controllers.

1   24.   (Previously Presented) The system of claim 1, wherein the plurality of

2   memory controllers are connected to the memory bus.

1   25.   (Previously Presented) The system of claim 1, wherein one of the at least

2   two memory controllers is adapted to generate its memory request on the memory bus

3   before data is returned for the memory request of the other one of the at least two

4   memory controllers.

1   26.   (Currently Amended) The system of claim 10, wherein at least two of the

2   memory controllers are adapted to generate concurrently pending memory requests on the

3   first memory bus, each of the concurrently pending memory requests comprising control

4   information and memory address information.

1   27.   (Currently Amended) The system of claim 26, wherein one of the at least

2   two memory controllers is adapted to generate its memory request including control

3   information and memory address information on the memory bus before data is returned

4   for the memory request of the other one of the at least two memory controllers.

1   28.   (Currently Amended) The method of claim 15, wherein generating the

2   requests on the memory bus comprises at least two of the memory controllers generating

3   concurrently pending requests on the memory bus, each of the concurrently pending

4   requests comprising control information and memory address information.

1   29.   (Currently Amended) The method of claim 28, wherein generating

2   concurrently pending requests comprises one of the at least two memory controllers

3   generating its request including control information and memory address information on

4   the memory bus before data is returned for the request of the other of the at least two

5   memory controllers.

1   30.   (Previously Presented) The article of claim 23, wherein the memory

2   controllers are connected to the memory bus.

1   31.   (New) The system of claim 1, wherein the predetermined priority scheme

2   enables the memory controllers to gain access to the memory bus without having to assert

3   arbitration requests.

1   32.   (New) The system of claim 1, wherein the memory controllers are adapted

2   to access the memory bus according to a round-robin priority scheme.

1   33.   (New) The system of claim 1, wherein the memory bus comprises a first

2   memory bus, the system further comprising:

3   a hub connected to the first memory bus; and

4   a second memory bus connected to the hub, at least two of the memory

5   controllers adapted to generate concurrently pending memory requests on the second

6   memory bus through the hub.

1   34.   (New) The system of claim 33, wherein each of the memory requests

2   comprises control information and memory address information, the at least two memory

3   controllers adapted to generate concurrently pending memory requests on the second

4   memory bus by providing control information and memory address information of the

5   concurrently pending memory requests on the second memory bus.

1   35.   (New) The system of claim 33, wherein each of the memory requests

2   comprises control information and memory address information, the at least two memory

3   controllers adapted to generate concurrently pending memory requests on the first

4   memory bus by providing control information and memory address information of the

5   concurrently pending memory requests on the first memory bus.

1   36.   (New) The system of claim 10, wherein the plurality of memory

2   controllers are each adapted to generate memory requests on the first one of the memory

3   buses, each memory controller to monitor memory requests on the first one of the

4   memory buses generated by another memory controller on the first one of the memory

5   buses.

1   37.   (New) The system of claim 10, wherein the plurality of memory

2   controllers are each adapted to generate memory requests on the second one of the

3   memory buses, each memory controller to monitor memory requests on the second one of

4   the memory buses generated by another memory controller on the second one of the

5   memory buses.

1   38.   (New) The system of claim 37, wherein the memory controllers are

2   adapted to access any of the memory buses according to a time slot priority scheme that

3   defines a plurality of time slots allocated to respective memory controllers.

1   39.   (New) The system of claim 38, wherein the memory controllers are

2   adapted to access any of the memory buses according to the time slot priority scheme

3   without asserting arbitration requests.

1   40.   (New) The system of claim 10, further comprising memory devices

2   connected to respective memory buses, the memory devices accessible by the memory

3   controllers.

1   41.   (New) The system of claim 11, wherein a first one of the memory

2   controllers is adapted to generate the read-modify-write transaction, the first one of the

3   memory controllers to assert a lock indication for a memory location accessed by the

4   read-modify-write transaction to prevent another one of the memory controllers from

5   accessing the memory location.

1   42.   (New) The method of claim 15, further comprising:

2   the plurality of memory controllers generating memory requests on a first

3   one of the memory buses; and

4   each memory controller monitoring memory requests on the first one of

5   the memory buses generated by another memory controller on the first one of the

6   memory buses.

1   43.   (New) The method of claim 15, further comprising:

2   the plurality of memory controllers generating memory requests on a

3   second one of the memory buses through the hub; and

4   each memory controller monitoring memory requests on the second one of

5   the memory buses generated by another memory controller on the second one of the

6   memory buses.

1   44.   (New) The article of claim 23, wherein generating memory requests on the

2   memory bus according to the time slot priority scheme is performed without generating

3   arbitration requests.